Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A digital audio volume control ~~An audio processing~~ circuit comprising:

a serial interface having an input for receiving a digital audio signal, and an output for serially outputting bits of the digital audio signal;

a shift register having a serial input connected to the output of the serial interface for storing bits of the digital audio signal;

a first-in-first-out (FIFO) buffer having a parallel input connected to a parallel output of the shift register;

a volume controller connected to the FIFO, the volume controller initiating loading of bits in the shift register into the FIFO according to a volume control signal; [[and]]

a digital-to-analog processor connected to a parallel output of the FIFO; and

an analog amplifier connected to an output of the digital-to-analog processor, the analog amplifier comprising an operational amplifier having a feedback variable resistance and an input variable resistance,

wherein the volume controller delays or speeds loading of bits in the shift register into the FIFO according to a coarse component of the volume control signal, and the volume controller adjusts the feedback variable resistance or the input variable resistance according to a fine component of the volume control signal.

2-4 (cancelled).

5 (currently amended): The digital audio volume control ~~audio processing~~ circuit of claim

1 wherein the volume controller is further connected to the digital-to-analog processor, and controls the output of the digital-to-analog processor to be a predetermined value when the volume control signal indicates a mute function.

6 (currently amended): An audio processing circuit comprising:

a serial interface having an input for receiving a digital audio signal, and an output for serially outputting bits of the digital audio signal;

a shift register having a serial input connected to the output of the serial interface for storing bits of the digital audio signal;

a first-in-first-out (FIFO) buffer having a parallel input connected to a parallel output of the shift register;

a volume controller connected to the FIFO, the volume controller initiating loading of bits in the shift register into the FIFO according to a volume control signal;

a digital-to-analog processor connected to a parallel output of the FIFO; and

an analog amplifier connected to an output of the digital-to-analog processor, the analog amplifier comprising an operational amplifier having a feedback variable resistance and an input variable resistance;

wherein the volume controller delays or speeds loading of bits in the shift register into the FIFO according to a coarse component of the volume control signal, and the volume controller adjusts the feedback variable resistance or the input variable resistance according to a fine component of the volume control signal.

7 (original): The audio processing circuit of claim 6 wherein the volume controller is further connected to the digital-to-analog processor, and controls the output of the digital-to-analog processor to be a predetermined value when the volume control signal indicates a mute function.

8 (currently amended): A method for adjusting the volume of a digital audio signal

comprising:

serially receiving bits of the digital audio signal;

setting a loading delay according to a coarse component of a volume control signal;

in parallel, forwarding a segment of the received bits at the expiry of the loading delay; [[and]]

processing the segment of bits into an analog audio signal, wherein the positions of the bits in the segment are directly related to the volume of the analog audio signal; and

receiving a fine component of the volume control signal and accordingly attenuating or amplifying the analog audio signal by an amount less than a unit attenuation or amplification resulting from a minimum adjustment of the loading delay.

9 (original): The method of claim 8 wherein setting the loading delay comprises lengthening the loading delay to right shift the bits of the segment thereby attenuating the analog audio signal, and shortening the loading delay to left shift the bits of the segment thereby amplifying the analog audio signal, when the serial receiving of bits for the segment is by decreasing order of significance.

10 (original): The method of claim 8 wherein setting the loading delay comprises lengthening the loading delay to right shift the bits of the segment thereby amplifying the analog audio signal, and shortening the loading delay to left shift the bits of the segment thereby attenuating the analog audio signal, when the serial receiving of bits for the segment is by increasing order of significance.

11 (cancelled).

12 (original): The method of claim 8 wherein processing the segment of bits comprises

setting each bit of the segment to a predetermined value when the volume control signal indicates a mute function.